Generalized Phase-Shift PWM for Active-Neutral-Point-Clamped Multilevel Converter

Yuzhuo Li, *Student Member, IEEE*, Hao Tian, *Member, IEEE* and Yun Wei Li, *Senior Member, IEEE*

***Abstract*—The multilevel active-neutral-point-clamped (ANPC) converters have more control freedoms compared to the conventional neutral-point-clamped topology due to increased switching redundancies. However, the device utilization of level-shift PWM is inherently low, and the scalability of space-vector-based PWM is challenging to realize for high-level (e.g., four-level or five-level) topologies. In this paper, a novel phase-shift PWM and the design approach for ANPC converter is proposed to handle these two problems simultaneously. The proposed idea enables the modular Phase-shift PWM design based on the switch group concept. In such a way, the complexity in the PWM design process can be significantly reduced with enhanced scalability for both the general and simplified ANPC topologies. Moreover, compared with conventional level-shift PWM, the proposed PWM schemes can fully utilize the devices for better loss distribution and higher equivalent switching frequency. Study cases have been done regarding output features, device utilizations, loss distributions, etc, through experimental verification and thorough discussions.**

***Index Terms*—Active-neutral-point-clamped converter, multilevel pulse-width modulation, phase-shift pulse-width modulation.**

I. Introduction

VOLTAGE-source multilevel converters have been widely implemented for different industrial applications, such as reactive power compensation, high-voltage direct-current transmission, wind energy conversion, and railway traction [1]-[2]. Among various topologies as shown in **Fig. 1**, active-neutral-point- clamped (ANPC) based converters feature some favorable advantages over conventional neutral-point-clamped (NPC) converters, such as: (1) the potential to obtain better loss distribution due to the large number of redundant switching states, (2) fault-tolerant capability even with multiple failure switches, (3) flexible device selection (e.g. hybrid Si+SiC bridges to improve converter performance with reasonable cost) [3]-[13]. In literature, two types of ANPC-based converters were introduced: one is the ANPC topology without flying capacitors (FCs) (in this paper, it is referred to as ANPC converter as shown in **Fig. 2**), the other is modified from ANPC topology with combination of FC legs (to avoid confusion, it is referred to as hybrid-clamped converter as shown in **Fig. 2**). Promising potentials of these converters (from three-level to nine-level topologies) have been demonstrated in recent research works towards various applications, such as medium voltage drive system, PV integration, battery management, and so on [9]-[12]. This paper focuses on ANPC converters. The ANPC topology is scalable, which means it is easy to design converters with an expected number of output levels [10]. Meanwhile, it does not need a floating capacitor balancing control or pre-charging as no flying capacitor is used in ANPC topology [5]. Although the device number will be increased for a high-level ANPC converter, it provides high design freedom that NPC or hybrid-clamped topology cannot possess [13].

For multilevel converters, especially when output level number is higher than three, carrier-based PWM schemes, i.e., level shift (LS) and phase shift (PS) PWM, are much easier to implement than space vector modulation (SVM) methods [7]-[19]. While conventional LS PWM tends to cause unequal loss distribution [3], [13]. An alternative method is to develop PS PWM which has been successfully applied for state-of-art topologies to achieve higher equivalent switching frequency (ESF), better device utilization, and evenly loss distribution [1], [18]. Recently, a hybrid PWM scheme has been applied in hybrid-clamped converters [11]-[12], [16]. The converter is controlled by a 3L PS PWM for FC legs and low switching frequency modulation for a 3L ANPC converter. However, it cannot be applied for ANPC converter since no FC legs exist in ANPC converters. For the conventional PS PWM schemes of cascaded H-bridge or modular multilevel converter, they utilize the inherent modular structures and generate the phase-shifted PWM signals for each submodule [18]. Due to the different topology operation principles and the lack of submodule structures, such methods cannot be implemented for ANPC converter as well [10], [13]. In [19], a PWM scheme with phase-shifted carriers was proposed for the three-level ANPC converter. A similar method was also introduced in [20] for the sub-topology of a three-level ANPC-based topology.

In summary, only a few carrier-based PWM or SVM are developed mainly for three-level ANPC converter [21], the generalized PS PWM schemes and the feasible design method for ANPC converter have not been developed yet.

Manuscript received June 12, 2019; revised September 24, 2019 and November 7, 2019; accepted November 18, 2019. This work was supported by the Natural Sciences and Engineering Research Council of Canada (NSERC) and Future Energy Systems (FES) funding from the Canada First Research Excellence Fund (CFREF). (Corresponding author: Hao Tian.)

The authors are with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB T6G 2R3, Canada (e-mail: yuzhuo@ualberta.ca; htian2@ualberta.ca; yunwei.li@ualberta.ca).

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2956372, IEEE Transactions on Industrial Electronics

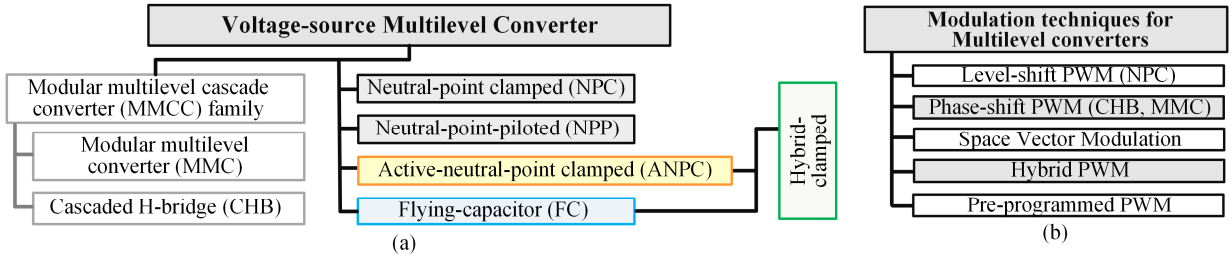


Fig.1 Classification of (a) voltage-source multilevel converters, (b) modulation techniques for multilevel converters based on [1]-[2].

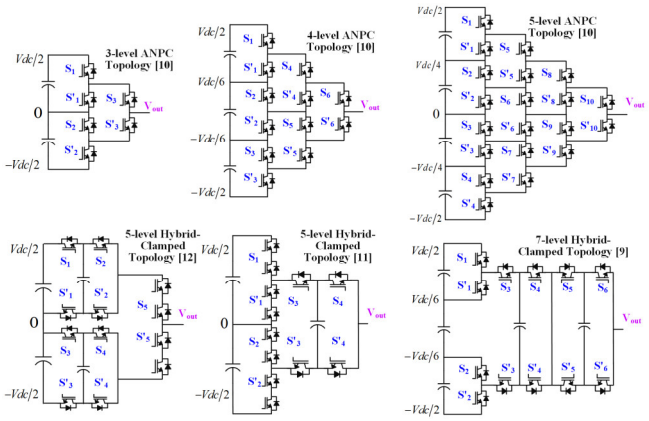


Fig.2 Topologies of the general 3L/4L/5L ANPC converters and three hybrid-clamped converters [9]-[12].

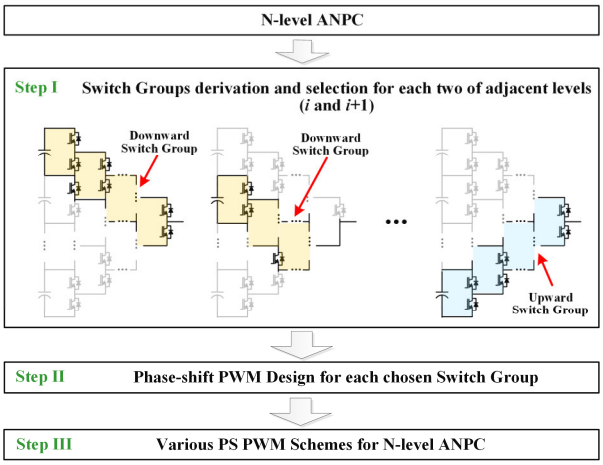


Fig.3 Phase-shift PWM Design Process for ANPC Converter.

In this paper, a general PS PWM scheme and the design approach are proposed for ANPC converters. To simplify the design process, the ANPC topology is modularly decomposed into several sub-topologies with their own PWM schemes. Each sub-topology, defined as a switch group in this paper, can operate independently to generate different output levels. Although the ANPC topology structure can be quite complicated when the voltage level increases, the PWM design for decomposed switch groups are maintained to be simple and easy to implement. Moreover, an (n+1)-level PWM can be directly synthesized through n-level schemes, which largely reduce the design complexity. So the scalability and modularity of the PWM design procedure can be guaranteed. Moreover, the designed PS PWM schemes can naturally achieve more evenly utilization of devices with better loss distribution and a higher ESF. In summary, this work is aiming at the unified PS PWM method, which has the following advantages:

(1) enhanced scalability and modularity,

(2) the simple design process for ANPC topology which can also be extended for simplified ANPC topology,

(3) higher device utilization and higher equivalent switching frequency,

(4) light computation burden for digital controllers.

It is worth noting that the balancing of DC-link capacitors shall be considered in practice for ANPC topologies. Diode front-end or balancing circuit can be used to clamp the DC voltages [22]-[23]. Also, the proposed PWM can be combined with the signal injection method to suppress the DC unbalance [24]. Since this paper is focused on the PS PWM design method to achieve better device utilization and higher ESF, to investigate the intrinsic modulation process without the effect of DC oscillations, all DC links are clamped through DC power supplies.

In the following Section II, the details of proposed methods and demonstration examples of designed PS PWM schemes are presented. The generalization of the proposed method for n-level ANPC converter is introduced in Section III. The feasibility of this method is verified by experiment results in Section IV. At last, the conclusions are drawn in Section V.

II. Proposed Generalized Phase-shift PWM Scheme with The Design Examples of ANPC Multilevel Converter

A. Phase-shift PWM design process for ANPC converter

Two main objectives of the proposed PS PWM are focused on: (1) simplify the design process through several modular steps, (2) achieve higher ESF through best utilization of switching devices. To realize the above goals, the three-step PS PWM design procedure is proposed and shown in **Fig. 3**.

Step I-Derive the switch groups: Sub-topologies named Switch Groups (SGs) for every two adjacent levels (i.e., the i^{th} and $(i+1)^{th}$ level, i is an integer) are derived and selected for ANPC topology. As shown in **Fig. 3**, two types of SGs can be found: downward SG and upward SG. Inside an SG, each half-bridge can be considered as a *Stage*.

Step II-Design PS PWM for each SG: PS PWM can be designed for each SG by utilizing interleaved carriers. Each carrier is corresponding to a stage.

Step III-Combine SG PWM schemes: All the designed PWM for SGs are combined as the final PWM scheme to operate the ANPC converter. In the following subsections, 3/4/5-level examples will be illustrated to describe the design details.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2956372, IEEE Transactions on Industrial Electronics

B. Phase-shifted PWM for switching groups

Based on the proposed design method, an ANPC converter can be considered as combinations of different SGs regards different output regions, which naturally decomposes the converter in terms of different operation points. In general, for ANPC converter with *i*-level outputs ($i \leq 5$), e.g., 3L, 4L, 5L in **Fig. 2**, there are three different types of upwards SGs (see **Fig. 4(a)** and **Fig. 5**) and three different types of downwards SGs (see **Fig. 6**). Inspired by the double frequency PWM schemes [19]-[20], a novel PWM scheme can be designed for each SGs to achieve the phase-shifted modulation.

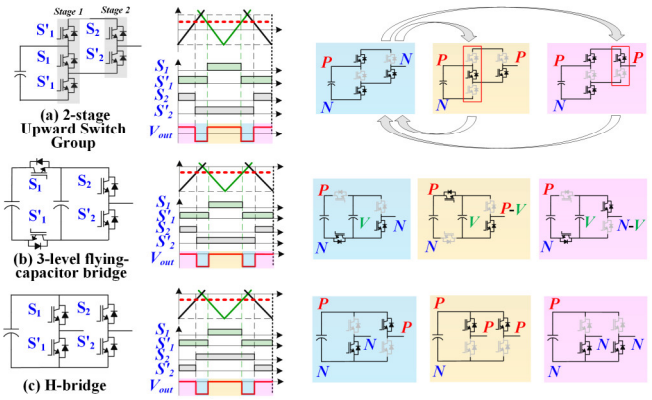


Fig.4 Phase-shifted PWM for (a) 2-stage upward switch group, (b) 3-level flying-capacitor bridge, (c) conventional H-bridge.

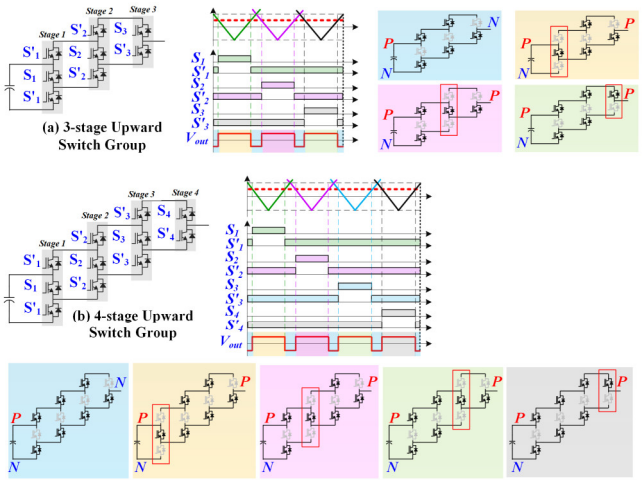


Fig.5 Phase-shifted PWM for (a) 3-stage upward switch group, (b) 4-stage upward switch group.

For 2-stage upward SG in **Fig. 4 (a)**, the PWM scheme is the same with the method in [20], where two carriers are phase-shifted by 180° and are utilized to compare with reference to operate five switches in this SG. As indicated by the arrows in Fig.4 (a), during different periods of one fundamental cycle, the switches in the corresponding SG will be turned ON and OFF while the states of other switches keep unchanged. In other words, SGs will take turns to make switching actions in one fundamental cycle and switching loss can be well distributed. The same carriers and same output waveforms can also be found in PS PWM schemes for 3-level FC bridge and conventional H-bridge [17]-[18], however, device utilizations are different as shown in **Fig. 4(b)** and **(c)**, respectively.

For 3-stage upward SG in **Fig. 5(a)**, three carriers are phase-shifted by 120° to modulate the eight switches in this SG. There are four switching states that will be generated in PS PWM and result in a triple ESF of output pulses. For a 4-stage upward SG, four carriers are used with 90° phase shift and result in four times ESF of output pulses in theory. Similar algorithms can also be developed for downward SGs, as shown in **Fig. 6**.

For each SG with the proposed PS PWM scheme, the PWM waveforms with increased ESF can be guaranteed as indicated in **Fig. 4~6**. And the same phenomenon also happens in the FC bridge and H-bridge scenarios with the same PS PWM logic but different switching states [16]-[18].

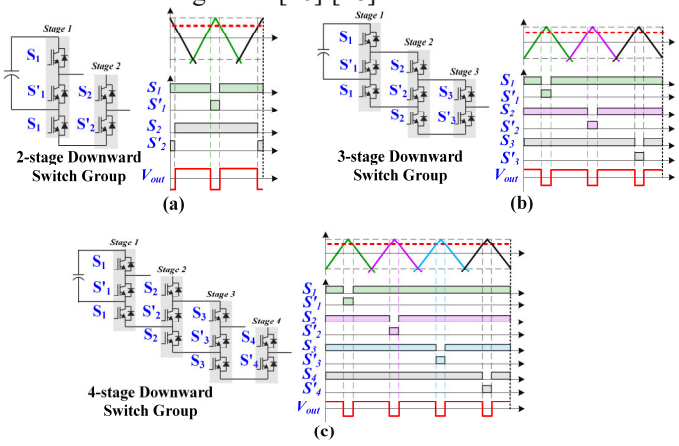


Fig.6 Phase-shifted PWM for (a) 2-stage downward switch group, (b) 3-stage downward switch group, (c) 4-stage downward switch group.

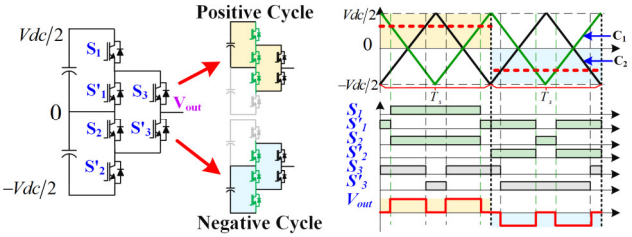


Fig.7 Phase-shift PWM for 3-level ANPC Converter.

C. 3-level PS PWM for ANPC converter

To better understand the proposed PS PWM design method, a 3-level ANPC converter is demonstrated first. In [19], the PWM schemes with the phase-shifted process is proposed to realize natural doubling of the inverter frequency. Such PWM was verified to have a better balancing of loss distribution in a 3-level ANPC converter with LS PWM. The theoretical gating signals are shown in **Fig. 7**. The scheme can be easily synthesized through the proposed PS PWM method.

Step I: Based on the concept of *Switch Group*, the 3-level ANPC has only two available SGs as shown in Fig.3, one is downward that produces an output voltage from $V_{dc}/2$ to 0, the other is upward that produces output voltage potentials from 0 to $-V_{dc}/2$.

Step II: PS PWM schemes are designed for these SGs, respectively. In positive half-cycle, associated switches (S_1, S'_1, S_2, S_3, S'_3) of downward SG are utilized. Two carriers (C_1 and

C_2) are phase-shifted by 180º, as shown in **Fig. 7**. The carrier frequency is f_{s1} for downward SG, while the ESF is $2f_{s1}$. In negative half-cycle, associated switches (S'_1, S_2, S'_2, S_3, S'_3) of upward SG are utilized. The same carriers can still be implemented with the same ESF.

Step III: two developed SG PWM schemes are implemented for positive and negative half-cycle, respectively. The unused switches during each half-cycle (S_1, S'_2) are controlled to be OFF to bearing the dc-link voltage properly, as shown in **Fig. 7**.

D. The proposed phase-shifted PWM for the general 4-level ANPC converter

Based on the PS PWM for SGs, the general 4-level ANPC can be modulated through the different combinations of SGs with designed PWM schemes in **Fig. 4~6**.

Step I: Proper SGs can be selected as shown in **Fig. 8** (in the Appendix, the complete list of SGs are provided). Eight associated switches (S_1, S'_1, S_2, S_4, S'_4, S_5, S_6, S'_6) are utilized to form downward SG #1, which has three stages. As the stages of derived SGs increase, the ESF increases as well, which guarantees power quality of phase voltage using lower switching frequency compared to conventional LS PWM. To achieve the highest ESF, downward SG #1 and #2 can be chosen for positive half-cycles. Based on the same idea, upward SG #1 and #2 can be chosen for negative half-cycles. The reason for two different SGs (downward SG#2, upward SG #1) during [-Vdc/6, Vdc/6] is to guarantee the symmetrical device utilization for [-Vdc/6, 0] and [0, Vdc/6]. If downward/upward SG #3 is chosen in this area, the device utilization will be different, while the output will be maintained the same.

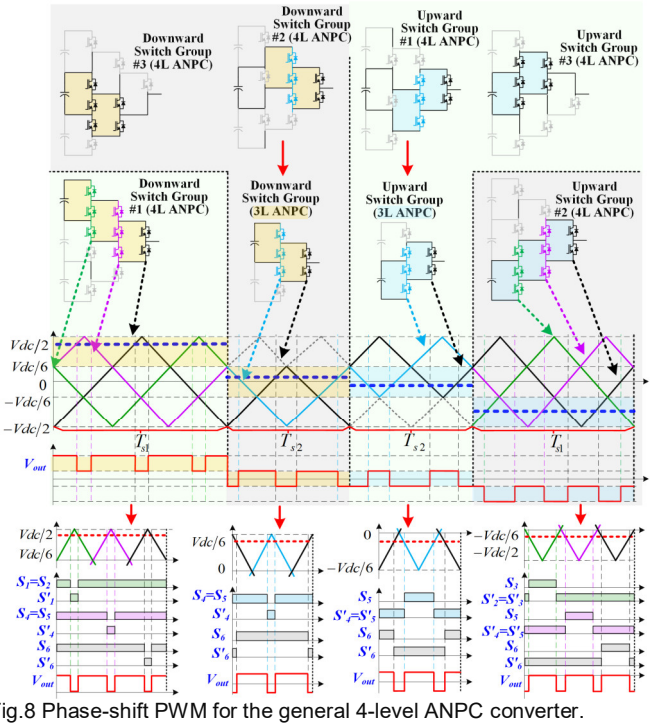


Fig.8 Phase-shift PWM for the general 4-level ANPC converter.

Step II: Based on **Fig. 6(b)**, the PS PWM for downward SG #1 utilizes three carriers which are phase-shifted by $1/(3f_{s1})$ (f_{s1} is the carrier frequency for downward SG #1, the ESF is $3f_{s1}$.) and compared with voltage reference. The PWM logic and generated gating signals are shown at the bottom of **Fig.8**. To output [0, V_{dc}/6], downward SG #2 is selected. Two carriers are shifted by $1/(2f_{s2})$ (f_{s2} is the carrier frequency for downward SG #2). The ESF is $2f_{s2}$. It can be seen the selected SG has the same form as a 3L case. Therefore, the 3L PS PWM schemes can be utilized for the 4L design case. The case of negative half-cycles is similar to that of positive half-cycles, which is omitted here.

Step III: All four PS PWM schemes for selected SGs are combined. For four different output regions, four carrier groups are enabled separately. In addition to the PWM switching signals, other switches in different output ranges are maintained fixed states, as indicated in **Fig. 8**: (1) during [Vdc/6, Vdc/2], switches [S_2', S_3', S_5'] are OFF and [S_3] are ON, (2) during [0, Vdc/6], [S_1, S_2, S_3, S_5'] are OFF and [S_1', S_2', S_3'] are ON, (3) during [-Vdc/6, 0], [S_1', S_2', S_3', S_4] are OFF and [S_1, S_2, S_3] are ON, (4) during [-Vdc/2, -Vdc/6], [S_1, S_2, S_4] are OFF and [S_1'] are ON.

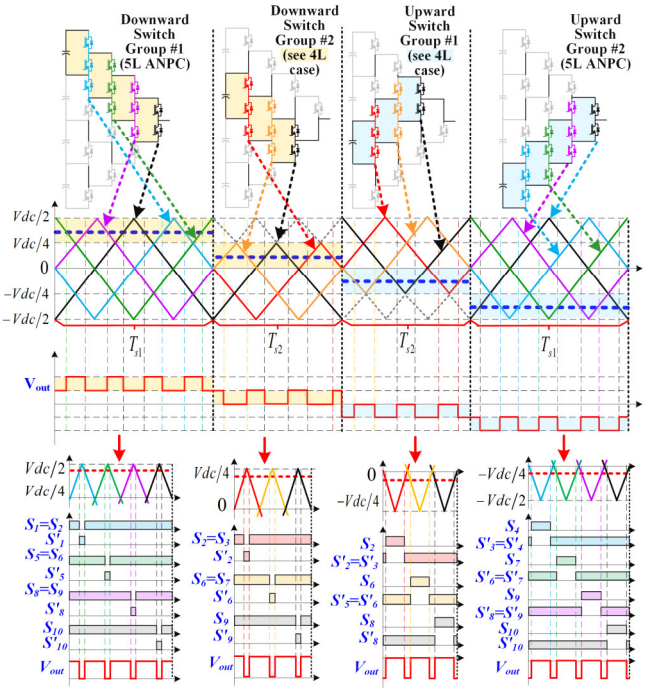


Fig.9 Phase-shift PWM for the general 5-level ANPC converter.

E. The proposed phase-shifted PWM for the general 5-level ANPC converter

PS PWM design for a 5L ANPC converter is taken as another example. There could be multiple possible choices of SGs in terms of different output regions (in the Appendix, the complete list of SGs are provided). To better utilize all the devices and achieve a high ESF, downward SG #1 and #2, upward SG #1 and #2 can be selected for four output regions, respectively.

Since the PS PWM schemes of these SGs have already been designed, the 5-level PS PWM can be simply derived with PWM of equivalent SGs in lower-level ANPC topologies, as indicated in **Fig. 9**. For example, the gating signals for S_2, S'_2, S_3 in downward SG #2 in **Fig. 9** are the same as S_1, S'_1, S_2 in downward SG #1 of the 4L case in **Fig. 8**. The corresponding PWM logic and generated outputs are also identical. Therefore, the complexity of the PS PWM design process is significantly

reduced.

Similar to the 4L case, during each region, only the selected SG is operated at PWM frequency, while the rest switches are maintained fixed states in 5L ANPC converter, as indicated in **Fig. 8**. For example, during [Vdc/4, Vdc/2], switches [S_2', S_3', S_4', S_6', S_7', S_9'] are OFF and [S_3, S_4, S_7] are ON.

III. Generalization for N-level ANPC Converter

Based on the previous examples, several principles are summarized for an *n*-level ANPC topology as the guidelines of the proposed design method in this section. The generalization of the design procedure is facilitated through the utilization of multiple lower-level schemes of SGs to control higher-level multilevel ANPC converters.

A. General design guidelines

The first step is the derivation of various SGs. Two guidelines should be followed:

Guideline 1 for Step I: ***Maximum stage number of the derived upward/downward SGs are selected*** for every two adjacent levels to have better utilization of all devices and achieve maximum ESF.

Guideline 2 for Step I: ***Derived SGs of n-level topology and an associated n-stage SG can be directly utilized*** to simplify the derivation process of (n±1)-level ANPC topology. Two possible derivations of (n+1)-level topology are demonstrated in **Fig. 10**. **Fig. 10(a)** shows the (n+1)-level topology realized by combing n-level topology with n-stage downward SG. **Fig. 10(b)** shows the (n+1)-level topology realized by using the same n-level topology with n-stage upward SG. The n−1 case is vice versa.

The second step is to design the associated PS PWM of derived SGs, which are summarized in **Fig. 11**. Two guidelines should be followed:

Guideline 3 for Step II: ***i carriers (C_1~C_i) are needed, and the phase-shift angle is 360°/i*** for i-stage upward (or downward) SG associated with output level $n-i$ and $n-i+1$ (or output level i and i+1). Each carrier is a triangle wave with frequency f_s and amplitude Vdc·i/(n−1).

Guideline 4 for Step II: ***The switching logic of the i^{th} carrier for upward/downward SG can be expressed as*:**

$$S_i = Sign(m_{ref} - C_i) \tag{1}$$

$$Sign(x) = \begin{cases} 1, & x > 0 \\ 0, & x \le 0 \end{cases} \tag{2}$$

where S_i is the switching function of the i^{th} switch, *Sign* is a symbolic function, m_{ref} denotes the modulated waveform.

The ESF f_{es} of the final carrier can be expressed as:

$$f_{es} = i * f_s \tag{3}$$

Note that the doubled frequency PWM for 3-level ANPC is the special case when i=2.

The third step is to combine different schemes of SGs to form the final designed PS PWM for ANPC topology, as shown in **Fig. 11(c)**. Two guidelines should be followed:

Guideline 5 for Step III: ***For every two adjacent levels, associated SGs can be selected based on the control objectives***, e.g., ESF, switching loss distribution, etc. During the design process of an n-level ANPC converter, there can be

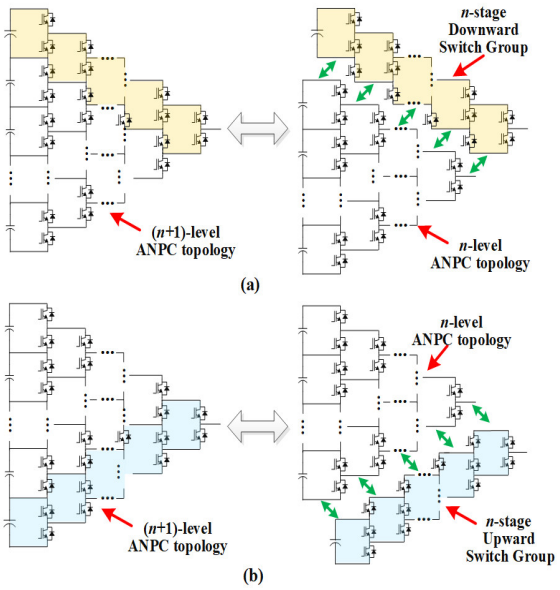


Fig.10 The derivation of (n+1)-level ANPC topology by an n-level circuit.

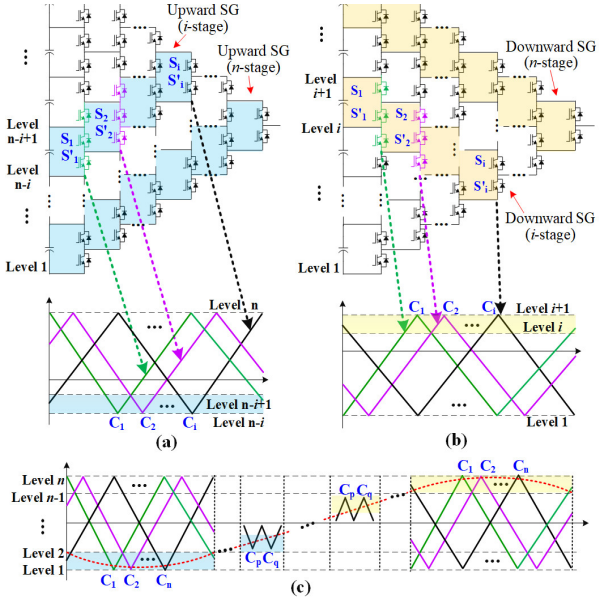


Fig.11 Phase-shift PWM designed for (a) upward switch groups, (b) downward switch groups, (c) the combined PWM of n-level ANPC topology with multiple carrier groups.

redundant SGs for the same output level range, such as downward SG #2 and #3 in 4-level converter example (**Fig. 8**) (in Appendix, more equivalent SGs are provided). Therefore, various PWM schemes can be derived based on different selections of SGs according to different requirements. This provides a wealth of control freedom for optimized PWM modulation to achieve complex control goals, such as: maximizing the ESF while maintaining the good switching loss balance as in 5L cases.

Guideline 6 for Step III: ***The reference wave is compared with carrier groups only in the corresponding level range*** to realize cooperation with multiple sets of carriers.

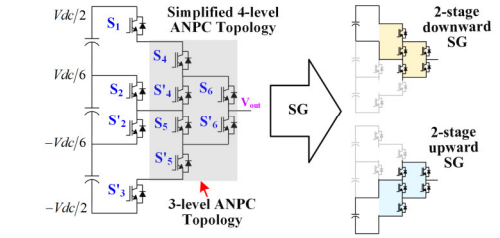
With the proposed approach, PS PWM for any ANPC converter can be systematically designed.

B. Design examples for simplified ANPC converters

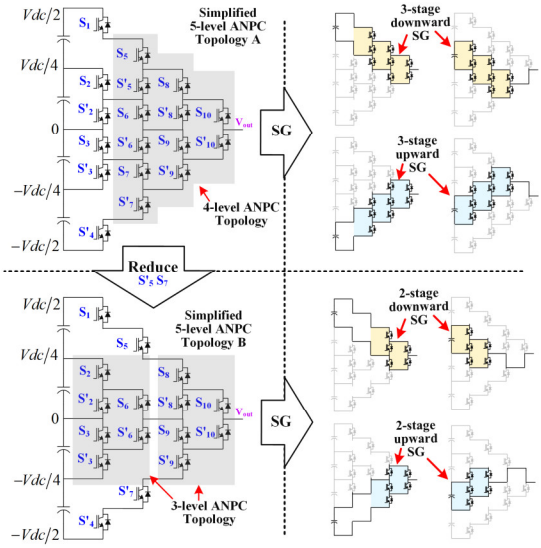
One of the major challenges of ANPC converters is the increased device number with high levels. Therefore, it could be cost-efficient to simplify the ANPC topology with a high-level output [25]. Recently, a matrix-model-based method is proposed in [26], which deals with this problem and provides several new simplified ANPC converters. Since the device numbers are smaller, the system cost will be reduced [27]. However, similar output performance can still be maintained.

Typically, the PWM schemes for simplified converters need redesign due to the redundant switching states, which is not easy to follow. Thanks to the enhanced scalability of the proposed method, the designed PS PWM schemes can be implemented for simplified ANPC converters in a more straightforward way. For example, a 4-level ANPC topology can be simplified as shown in **Fig. 12**. The converter has two 2-stage SGs, which can also be derived in a general 4-level ANPC converter. Therefore, the PS PWM of the 4-level case can be implemented easily. Similarly, two simplified 5-level ANPC converter (topology A and B in **Fig. 13**) can be derived, and the same types of 3-stage and 2-stage SGs in the 5-level case can be utilized as indicated in **Fig. 14**.

Recently, the extended multilevel active-clamped topology is also introduced in literature [5], which provides an alternative way of converter leg design for a wide range of voltage and current ratings (especially the high-power applications). The operation principles are essentially the same as the general ANPC converters, while the proposed PWM can also be implemented without changes.



(a) Examples of simplified 4-level ANPC converters



(b) Examples of simplified 5-level ANPC converters

Fig.12 PS PWM for simplified 4-level and 5-level ANPC converters.

IV. Experimental Verifications and Loss Analysis

A. Experimental results

To verify the ESF and power quality of the proposed PWM method, one 5L phase-leg is built for experiments with parameters listed in Table. I. The experimental setups are shown in **Fig. 13**. The measured switches are highlighted in blue shadows. To compare with PS PWM, three different LS PWM schemes are implemented based on the method in [13].

TABLE. I
EXPERIMENT PARAMETERS

Parameter	Value
Rated Phase Voltage (peak)	60 V
Rated Phase Power	500 VA
DC link Voltage	120 V
Carrier Frequency f_{c1} (PS PWM)	390 Hz
Carrier Frequency f_{c2} (PS PWM)	520 Hz
Carrier Frequency f_{c3} (LS PWM)	1560 Hz
Equivalent Switching Frequency	1560 Hz
Modulation Index	0.9 and 0.45
Line Frequency f_o	60 Hz
Load inductance	30 mH
Load resistance	27.5-2.7 Ω

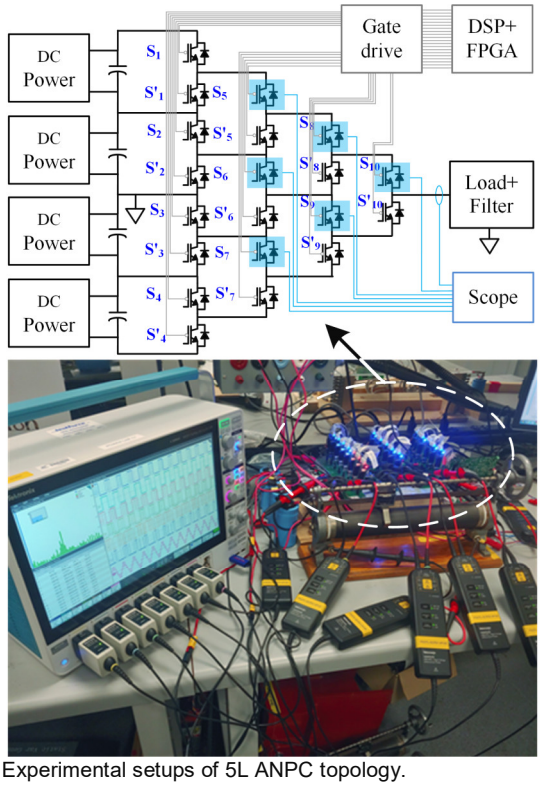


Fig.13 Experimental setups of 5L ANPC topology.

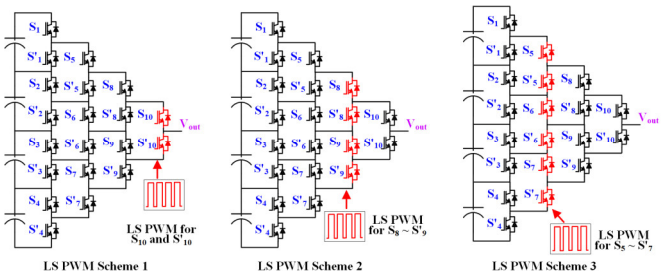


Fig.14 Three LS PWM schemes of the general 5L ANPC converter with different device utilizations.

They have three different utilizations of devices, as indicated

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2956372, IEEE Transactions on Industrial Electronics

in **Fig. 14**. In LS PWM scheme 1, the switches [S_{10}, S_{10}'] are utilized at f_{c3}, the rest switches operate at f_o. In LS PWM scheme 2, the switches [S_8, S_8', S_9, S_9'] are utilized at f_{c3}, the rest switches operate at f_o. In LS PWM scheme 3, the switches [S_5, S_5', S_6, S_6', S_7, S_7'] are utilized at f_{c3}, the rest switches operate at f_o. The experimental results verify such device utilization in **Fig. 15(a)~(d)** with different modulation index (0.9 and 0.45).

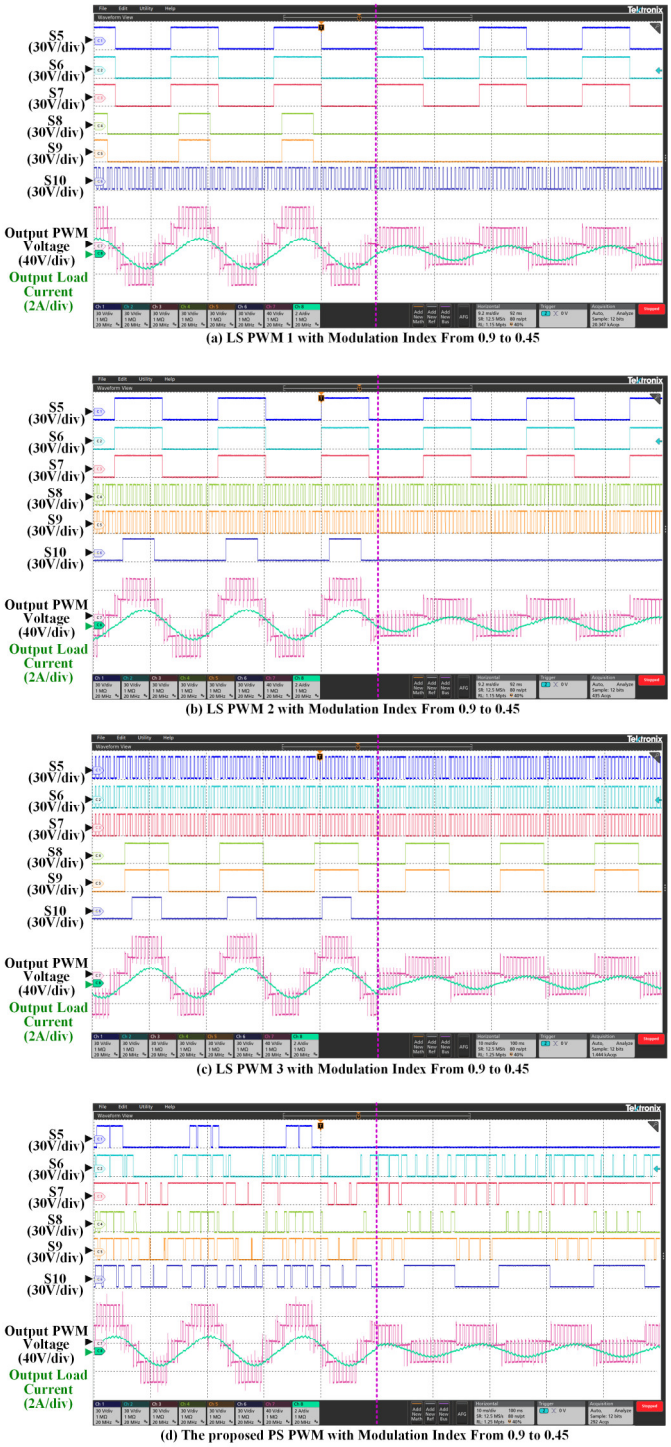


Fig.15 The gating signals of switches [S5, S6, S7, S8, S9, S10], output PWM waveforms and load current of the general 5L ANPC converter using different PWM methods: (a) LS PWM 1, (b) LS PWM 2, (b) LS PWM 3, (b) the proposed PS PWM. (Modulation index from 0.9 to 0.45)

The FFT analysis verifies that the ESF is three/four times the device frequency through the proposed PS PWM. The introduced low order harmonics are mainly because of double frequency ripples of single-phase configurations and the sideband of switching frequency harmonics, as shown in **Fig. 16**.

The different load conditions are also considered, as shown in **Fig. 17**, which shows the feasibility of the proposed method. The introduced fluctuation of DC links is mainly because of the increased power consumption in single-phase systems [28].

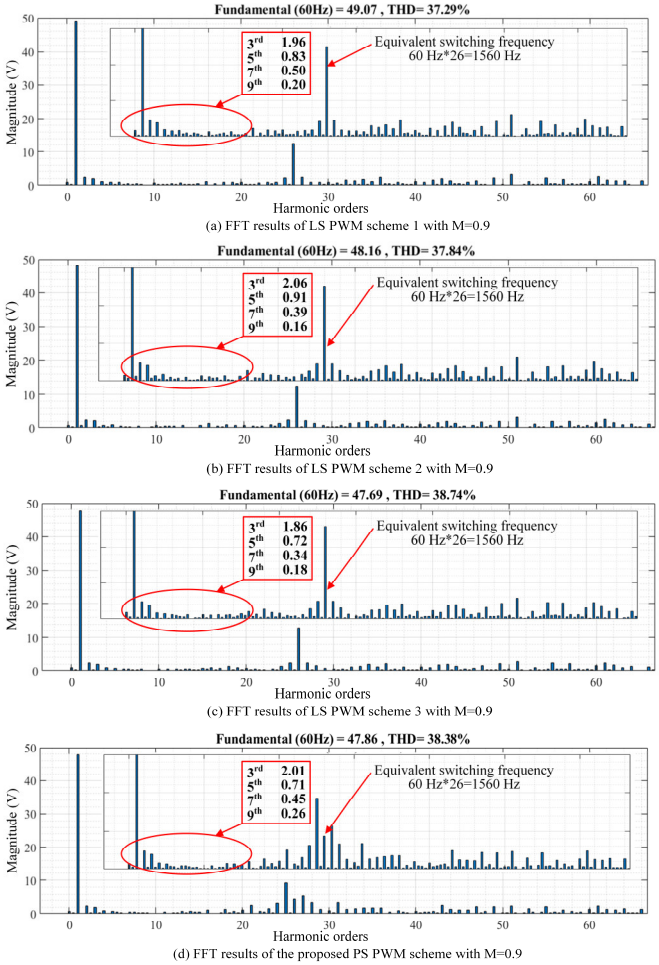


Fig.16 FFT analysis of different PWM methods: (a) LS PWM scheme 1, (b) LS PWM scheme 2, (c) LS PWM scheme 3, (d) the proposed PWM scheme.

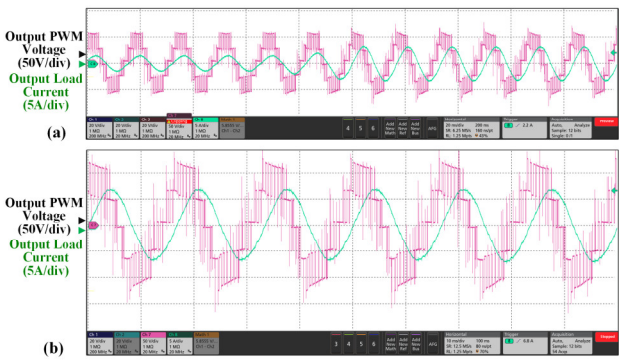


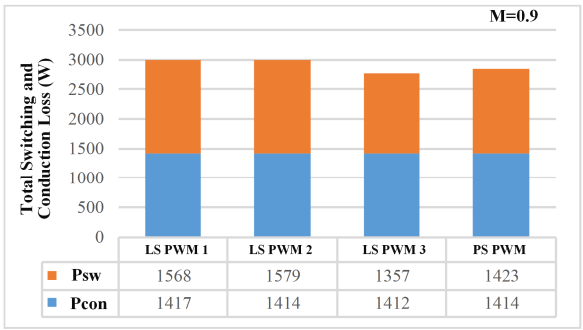
Fig.17 (a) The output PWM waveforms of load change from 30mH/27.5Ω to 30mH/2.7Ω. (b) increased output power with higher DC-link voltage.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2956372, IEEE Transactions on Industrial Electronics

B. Analysis of loss distribution

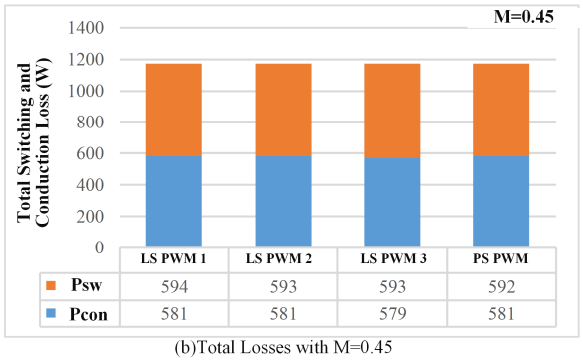
To demonstrate the loss distribution performance of the proposed PS PWM, the total/switching losses of 5L ANPC converter with 3300V 800A IGBT (i.e., Infineon FZ800R33KF2C) under same ESF (1560Hz) and modulation index (0.9 and 0.45) are chosen as an example through PLECS tools in MATLAB/Simulink.

The PS PWM is the same as **Fig. 8**. Three LS PWM schemes are the same with LSPWM methods used in experiments. The power factor, load current, and blocking voltages of devices are maintained the same. Both the conduction loss and switching loss of switches and diodes are considered based on the output characteristics curves and switching energy loss curves.



	LS PWM 1	LS PWM 2	LS PWM 3	PS PWM
Psw	1568	1579	1357	1423
Pcon	1417	1414	1412	1414

(a)Total Losses with M=0.9



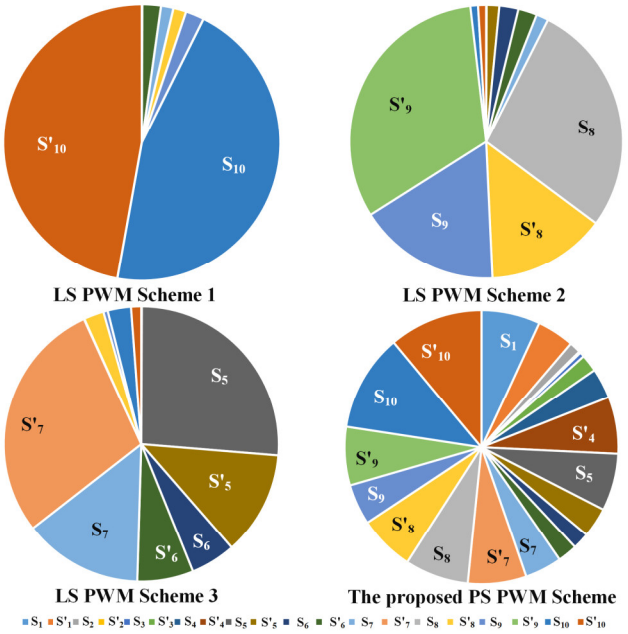
	LS PWM 1	LS PWM 2	LS PWM 3	PS PWM
Psw	594	593	593	592
Pcon	581	581	579	581

(b)Total Losses with M=0.45

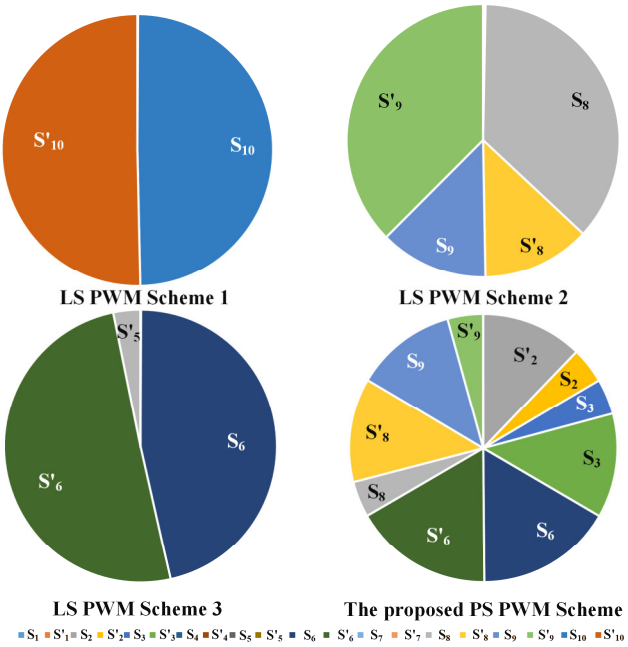
Fig.18 Total losses of four different PWM schemes with (a) modulation index is 0.9, (b) modulation index is 0.45.

Firstly, the total losses are investigated for these four schemes. Both the conduction losses and switching losses are listed in **Fig. 18**, where P_{sw} indicates switching power loses, P_{con} indicates conducting power loses. It turns out all these four methods have similar conduction losses. The slightly higher losses of LS PWM 1 and 2 with 0.9 modulation index are caused by their different commutation processes among the four PWM methods.

Secondly, the switching losses distributions are compared. All the switches in 5L ANPC converter are included, and their losses are shown in **Fig. 19**. In LS PWM, the switching losses are concentrated on a few switches, e.g., one or two switches can contribute to half of all switching losses. With the same ESF, the designed PS PWM can achieve better switching loss distribution than LS PWM schemes under both high and low modulation index. This is because the proposed PS PWM naturally distributes the switching actions evenly in each SGs.



(a) Switching Loss Distribution of Different PWM Methods with **M=0.9**



(b) Switching Loss Distribution of Different PWM Methods with **M=0.45**

Fig.19 Switching loss distributions of four different PWM schemes with (a) modulation index is 0.9, (b) modulation index is 0.45.

C. Summary

Based on experimental results and above analysis, the comparisons between the proposed PS PWM and three LS PWM schemes for ANPC converter are summarized in Table. II. Since the proposed method uses the carrier phase-shifted technique, ESF with multiple times of carrier frequency can be achieved. Under the same ESF, both the power quality and total power losses (conduction and switching losses) are similar among these four PWM schemes. However, due to inherent balanced switching actions within SGs, the proposed PS PWM features a much better switching loss distribution.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2956372, IEEE Transactions on Industrial Electronics

TABLE. II
SUMMARY OF THE PROPOSED PS PWM AND CONVENTIONAL LS PWM SCHEMES FOR ANPC CONVERTERS

	LS PWM Scheme 1	LS PWM Scheme 2	LS PWM Scheme 3	Proposed PS PWM
Equivalent Switching Frequency	Same as carrier frequency			Multiple times of carrier frequency
Power Quality	PS PWM has higher power quality if device/carrier frequency is the same with LS PWM; all schemes have a similar output power quality using the same equivalent switching frequency.			
Total losses	Similar total loss performance under same equivalent switching frequency			
Switching Loss distribution	Most uneven distributed	Uneven distributed	Uneven distributed	Much better distributed
Utilized Switches (at PWM frequency)	Two (five-level case)	Four (five-level case)	Six (five-level case)	All (five-level case)
Scalability	Can be utilized for any ANPC topologies	Can be utilized for any ANPC topologies	Can be utilized for ANPC topologies with more than three levels	Can be utilized for ANPC topologies with more than three levels

V. CONCLUSIONS

This paper proposes a general three-step PWM design method for the ANPC converter with a novel PS PWM. It is based on different operation principles from the conventional methods for flying-capacitor-based, cascaded H-bridge, or modular multilevel converter. With more evenly distributed switching actions among all devices, the designed PS PWM schemes feature better utilization of devices and higher ESF compared with conventional LS PWM. Moreover, high-level PWM schemes can be synthesized through low-level schemes. In such a way, the PS PWM design for ANPC topology can be realized modularly for both the general and the simplified ANPC converters. Besides, the extensibility and reduced computation burden make the proposed method very suitable for multi-level ANPC topologies (e.g., 4- and 5-level). The five-level PS PWM scheme is designed with experimental validation and thorough discussions and comparisons, which shows a better performance regards device utilization and loss distribution.

APPENDIX

A. Different switch groups for the general 4-level ANPC converter

For the 4L ANPC converter, the operation range is naturally divided into three parts based on the DC links. There can be as many as ***14*** different selections for the general 4-level ANPC converter based on *i*-stage SGs (*i*>1) as shown in **Fig. a**.

B. Different switch groups for the general 4-level ANPC converter

The operation range 5L ANPC converter is naturally divided into four parts. The selections using *i*-stage SGs (*i*>1) can be as many as ***46***. In **Fig. b**, for the sake of simplicity, the topology is indicated by abstract blocks with different colors. Yellow blocks represent the downward SGs, blue ones mean upward SGs, grey ones are not utilized switches during this output region.

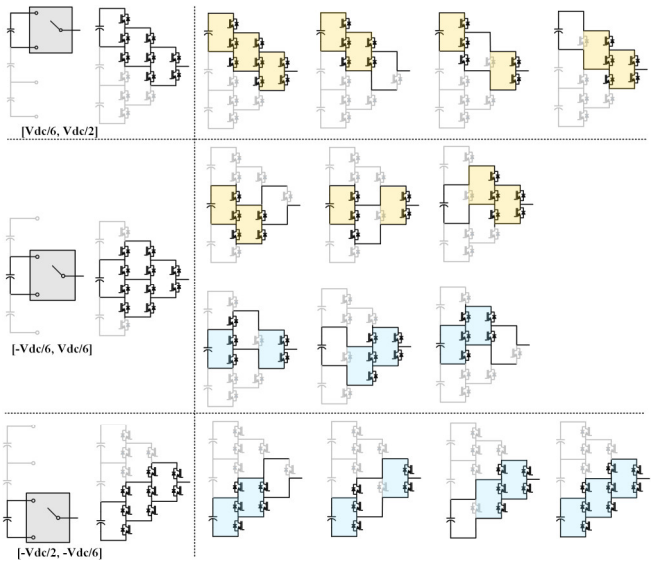


Fig. a. Possible operation patterns in terms of different switch group selections for the general 4-level ANPC converter.

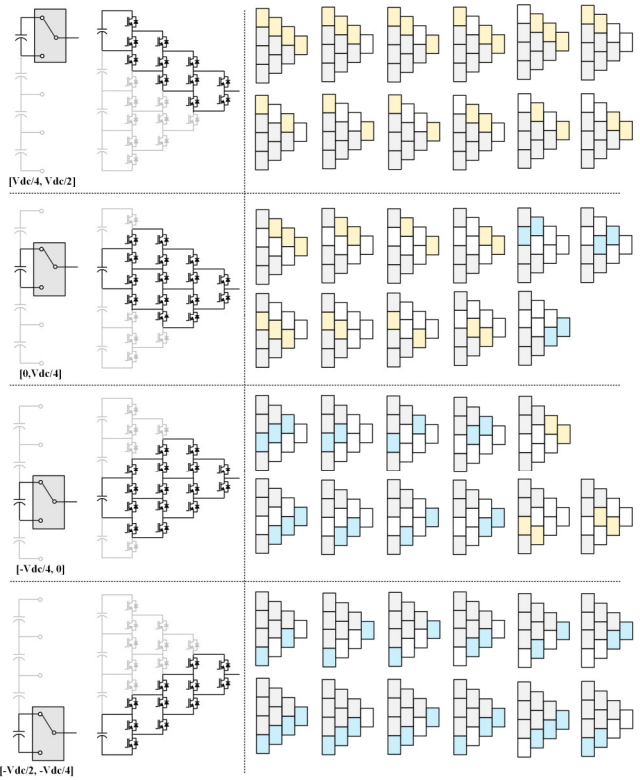


Fig. b. Possible operation patterns in terms of different switching group selections for the general 5-level ANPC converter.

C. Equivalent switch groups

Note that there is some SGs equivalent to each other in terms of output as demonstrated in **Fig. c**. For example, in **Fig. a**, three downward SGs in output region [-Vdc/6, Vdc/6]

(highlighted by dotted green rectangular) are equivalent to each other and can be modulated through the same schemes. The same truth can be found in the same region with three upward SGs highlighted by dotted brown rectangular.

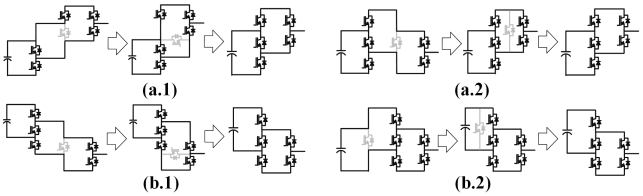


Fig. c. (a) Equivalent 2-stage upward switch groups, (b) Equivalent 2-stage downward switch groups.

REFERENCES

[1] J. I. Leon, S. Vazquez and L. G. Franquelo, "Multilevel Converters: Control and Modulation Techniques for Their Operation and Industrial Applications," in *Proceedings of the IEEE*, vol. 105, no. 11, pp. 2066-2081, Nov. 2017.

[2] H. Akagi, "Multilevel Converters: Fundamental Circuits and Systems," in *Proceedings of the IEEE*, vol. 105, no. 11, pp. 2048-2065, Nov. 2017.

[3] T. Bruckner, S. Bernet and H. Guldner, "The active NPC converter and its loss-balancing control," in *IEEE Transactions on Industrial Electronics*, vol. 52, no. 3, pp. 855-868, June 2005.

[4] J. Rodriguez, S. Bernet, P. K. Steimer and I. E. Lizama, "A Survey on Neutral-Point-Clamped Inverters," in *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2219-2230, July 2010.

[5] S. Busquets-Monge and L. Caballero, "Switching-Cell Arrays—An Alternative Design Approach in Power Conversion," in *IEEE Transactions on Industrial Electronics*, vol. 66, no. 1, pp. 25-36, Jan. 2019.

[6] S. Busquets-Monge *et al*., "Multi-Battery-Fed Neutral-Point-Clamped Dc-Ac Converter with SoC Balancing Control to Maximize Capacity Utilization," in *IEEE Transactions on Industrial Electronics*. 2019.(Early acess)

[7] P. Azer, S. Ouni and M. Narimani, "A Novel Fault-Tolerant Technique For Active Neutral Point Clamped Inverter Using Carrier-Based PWM," in *IEEE Transactions on Industrial Electronics*. 2019.(Early acess)

[8] C. Li *et al*., "Space Vector Modulation for SiC & Si Hybrid ANPC Converter in Medium Voltage High-Speed Drive System," in *IEEE Transactions on Power Electronics*. 2019. (*Early Access*)

[9] H. Tian and Y. Li, "An Active Capacitor Voltage Balancing Method for Seven Level Hybrid Clamped (7L-HC) Converter in Motor Drives," in *IEEE Transactions on Power Electronics*. 2019. (*Early Access*)

[10] S. Busquets-Monge and J. Nicolas-Apruzzese, "A Multilevel Active-Clamped Converter Topology—Operating Principle," in *IEEE Transactions on Industrial Electronics*, vol. 58, no. 9, pp. 3868-3878, Sept. 2011.

[11] K. Wang, L. Xu, Z. Zheng and Y. Li, "Capacitor Voltage Balancing of a Five-Level ANPC Converter Using Phase-Shifted PWM," in *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1147-1156, March 2015.

[12] R. Naderi, A. K. Sadigh and K. M. Smedley, "Dual Flying Capacitor Active-Neutral-Point-Clamped Multilevel Converter," in *IEEE Transactions on Power Electronics*, vol. 31, no. 9, pp. 6476-6484, Sept. 2016.

[13] Y. Li, Y. W. Li, H. Tian, N. R. Zargari and Z. Cheng, "A Modular Design Approach to Provide Exhaustive Carrier-Based PWM Patterns for Multilevel ANPC Converters," in *IEEE Transactions on Industry Applications*, vol. 55, no. 5, pp. 5032-5044, Sept.-Oct. 2019.

[14] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," in *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 858-867, Aug 2002.

[15] H. Tian and Y. W. Li, "Carrier-Based Stair Edge PWM (SEPWM) for Capacitor Balancing in Multilevel Converters With Floating Capacitors," in *IEEE Transactions on Industry Applications*, vol. 54, no. 4, pp. 3440-3452, July-Aug. 2018.

[16] C. Li, S. Wang, Q. Guan and D. Xu, "Hybrid Modulation Concept for Five-Level Active-Neutral-Point-Clamped Converter," in *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 8958-8962, Dec. 2017.

[17] J. I. Leon, S. Kouro, L. G. Franquelo, J. Rodriguez and B. Wu, "The Essential Role and the Continuous Evolution of Modulation Techniques for Voltage-Source Inverters in the Past, Present, and Future Power Electronics," in *IEEE Transactions on Industrial Electronics*, vol. 63, no. 5, pp. 2688-2701, May 2016.

[18] Y. Li, Y. Wang and B. Q. Li, "Generalized Theory of Phase-Shifted Carrier PWM for Cascaded H-Bridge Converters and Modular Multilevel Converters," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 2, pp. 589-605, June 2016.

[19] D. Floricau, E. Floricau, and M. Dumitrescu, "Natural doubling of the apparent switching frequency using three-level ANPC converter," in Proc. Int. School Nonsinusoidal Currents Compensation, Jun. 2008, pp. 1–6.

[20] Y. Gu, W. Li, Y. Zhao, B. Yang, C. Li and X. He, "Transformerless Inverter With Virtual DC Bus Concept for Cost-Effective Grid-Connected PV Power Systems," in *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 793-805, Feb. 2013.

[21] Y. Jiao, S. Lu and F. C. Lee, "Switching Performance Optimization of a High Power High Frequency Three-Level Active Neutral Point Clamped Phase Leg," in *IEEE Transactions on Power Electronics*, vol. 29, no. 7, pp. 3255-3266, July 2014.

[22] G. P. Adam, S. J. Finney, A. M. Massoud and B. W. Williams, "Capacitor Balance Issues of the Diode-Clamped Multilevel Inverter Operated in a Quasi Two-State Mode," in *IEEE Transactions on Industrial Electronics*, vol. 55, no. 8, pp. 3088-3099, Aug. 2008.

[23] Z. Shu, X. He, Z. Wang, D. Qiu and Y. Jing, "Voltage Balancing Approaches for Diode-Clamped Multilevel Converters Using Auxiliary Capacitor-Based Circuits," in *IEEE Transactions on Power Electronics*, vol. 28, no. 5, pp. 2111-2124, May 2013.

[24] Z. Pan and F. Z. Peng, "A Sinusoidal PWM Method With Voltage Balancing Capability for Diode-Clamped Five-Level Converters," in *IEEE Transactions on Industry Applications*, vol. 45, no. 3, pp. 1028-1034, May-june 2009.

[25] X. Yuan, "Derivation of Voltage Source Multilevel Converter Topologies," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 2, pp. 966-976, Feb. 2017.

[26] Y. Li, H. Tian and Y. W. Li, "Systematic Derivation of Simplified Active-Neutral-Point-Clamped Multilevel Converter through Matrix Models," *2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Toronto, ON, Canada, 2019, pp. 1-8.

[27] Z. Cheng and N. Zargari, " Sparse matrix multilevel actively clamped power converter," US Patent: US20160336872A1.

[28] Y. Sun, Y. Liu, M. Su, W. Xiong and J. Yang, "Review of Active Power Decoupling Topologies in Single-Phase Systems," in *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 4778-4794, July 2016.

Yuzhuo Li (S'15) received the B.S. degree and M.S. degree in Control Science and Engineering from Shandong University, China, in 2012 and 2015, respectively. Since 2015, he has been studying towards PhD degree in University of Alberta, Canada.

His main research interests are the systematic power converter topology derivation and PWM design.

Hao Tian (S'12--M'19) received the B.S. and M.Eng. degrees in electrical engineering from Shandong University, Jinan, China, in 2011 and 2014, respectively, and the Ph.D. degree in energy system from University of Alberta, Edmonton, Canada, in 2019. Since 2019, he has been working as a Postdoctoral Research Fellow with University of Alberta.

His research interests include multilevel topology and PWM, high-power converter

control, and power quality of hybrid AC-DC microgrid.

Yun Wei Li (S'04-M'05-SM'11) received the B.Sc. in Engineering degree in electrical engineering from Tianjin University, Tianjin, China, in 2002, and the Ph.D. degree from Nanyang Technological University, Singapore, in 2006.

In 2005, Dr. Li was a Visiting Scholar with Aalborg University, Denmark. From 2006 to 2007, he was a Postdoctoral Research Fellow at Ryerson University, Canada. In 2007, he also worked at Rockwell Automation Canada before he joined University of Alberta, Canada in the same year. Since then, Dr. Li has been with University of Alberta, where he is a Professor now. His research interests include distributed generation, microgrid, renewable energy, high power converters and electric motor drives.

Dr. Li serves as Editor-in-Chief for IEEE Transactions on Power Electronics Letters. Prior to that, he was Associate Editor for IEEE Transactions on Power Electronics, IEEE Transactions on Industrial Electronics, IEEE Transactions on Smart Grid, and IEEE Journal of Emerging and Selected Topics in Power Electronics. Dr. Li received the Richard M. Bass Outstanding Young Power Electronics Engineer Award from IEEE Power Electronics Society in 2013 and the second prize paper award of IEEE Transactions on Power Electronics in 2014.